Notice of Allowability	Application No.	Applicant(s)	
	10/602,716	MOULI, CHANDRA	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *06/11/2007*.

2. ☒ The allowed claim(s) is/are *1-23,25-71 and 73-77*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/11/2007 has been entered.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Gianni Minutoli Registration No. 41,198 on 09/04/2007.

The application has been amended as follows:

1. (Currently amended) A pixel cell comprising:

a photo-conversion device;

a sensing node; and

a first transistor for gating charge from said photo-conversion device to said sensing node; said first transistor comprising a gate electrode having a length ~~and a width,~~ and a channel region under said gate electrode,

said ~~width~~ length of said gate electrode extending from said photo-conversion device to said sensing node,

said length of said gate electrode being divided into a plurality of gate electrode regions, each gate electrode region extending from said photo-conversion device to said sensing node, wherein at least one said gate electrode region has a work-function greater than a work-function of n+ Si, and another said gate electrode region has a different work-function from that of said at least one gate electrode region,

said channel region comprising respective portions below each gate electrode region, wherein a doping concentration of at least one portion of said channel region is determined in part by the work-function of the respective gate electrode region.

2. (Original) The pixel cell of claim 1, wherein the first transistor is a transfer transistor for transferring photo-generated charge from the photo-conversion device to a floating diffusion region.

3. (Previously presented) The pixel cell of claim 1, wherein at least one gate electrode region comprises a mid-gap material.

4. (Original) The pixel cell of claim 3, wherein the mid-gap material is selected from the group consisting of: $Si_{1-x}Ge_x$, TiN/W, Al/TiN, Ti/TiN, and TaSiN.

5. (Original) The pixel cell of claim 3, wherein the mid-gap material is $Si_{1-x}Ge_x$ and wherein the mole fraction of Ge in the $Si_{1-x}Ge_x$ is approximately 0.4.

6. (Previously presented) The pixel cell of claim 5, wherein the at least one gate electrode region is doped to one of a first or second conductivity type.

7. (Previously presented) The pixel cell of claim 1, wherein at least one gate electrode region comprises a degenerately doped p+ polysilicon layer.

8. (Previously presented) The pixel cell of claim 1, wherein at least one gate electrode region comprises a layer of lower doped polysilicon of a first or second conductivity type.

9. (Previously presented) The pixel cell of claim 8, wherein at least one gate electrode region has a dopant profile allowing for at least partial depletion of the at least one gate electrode region.

10. (Original) The pixel cell of claim 8, wherein the dopant is indium.

11. (Original) The pixel cell of claim 1, wherein there is approximately no active dopant in at least one portion of the channel region.

12. (Previously presented) The pixel cell of claim 1, further comprising:

a second transistor formed adjacent said sensing node, wherein the second transistor comprises a gate electrode, the gate electrode comprising at least one gate electrode region having a work-function greater than a work-function of n+ Si.

13. (Previously presented) The pixel cell of claim 12, wherein at least one second transistor gate electrode region is formed of a same material as the at least one gate electrode region.

14. (Currently amended) The pixel cell of claim 1, wherein the at least one said gate electrode region is a first gate electrode region and the another said gate electrode

region is a second gate electrode region and the first transistor comprises ~~first and second gate electrode regions and~~ first and second channel portions under the first and second gate electrode regions, respectively.

15. (Previously presented) The pixel cell of claim 14, wherein each of the first and second gate electrode regions extends over an active area by a different distance.

16. (Previously presented) The pixel cell of claim 14, wherein the first and second gate electrode regions have different work-functions, and wherein each work-function is greater than a work-function of n+ Si.

17. (Previously presented) The pixel cell of claim 14, wherein the first and second gate electrode regions comprise a same material having different doping characteristics.

18. (Currently amended) The pixel cell of claim 1, wherein the at least one said gate electrode region is a first gate electrode region and the another said gate electrode region is a second gate electrode region and the first transistor comprises ~~first, second, and~~ a third gate electrode regions extending from said photo-conversion device to said sensing node and first, second, and third channel portions under the first, second, and third gate electrode regions, respectively.

19. (Previously presented) The pixel cell of claim 18, wherein the first gate electrode region is between the second and third gate electrode regions, and wherein the second and third gate electrode regions are each over a respective area where an isolation region and an active region meet, and wherein at least one of the second and third gate electrode regions has a work-function greater than a work-function of n+ Si.

20. (Previously presented) The pixel cell of claim 19, wherein the second and third gate electrode regions have a same work-function.

21. (Previously presented) The pixel cell of claim 19, wherein the doping concentration of at least one of the second and third channel portions is determined at least in part by the work-function of the respective gate electrode region.

22. (Previously presented) The pixel cell of claim 19, wherein the first gate electrode region is formed of a different material than the second and third gate electrode regions.

23. (Previously presented) The pixel cell of claim 19, wherein the first, second, and third gate electrode regions are formed of a same material having different doping characteristics.

24. (Canceled)

25. (Previously presented) A pixel cell comprising: a photo-conversion device at a surface of a substrate; and a transistor formed over a substrate and adjacent to the photo-conversion device, the transistor comprising a gate electrode overlying a channel region, the gate electrode having a length extending from a source/drain region to the photo-conversion device and the gate electrode comprising at least two gate electrode regions, each gate electrode region extending the length of the gate electrode and having a substantially uniform dopant type and concentration, wherein at least one of the gate electrode regions has a work-function greater than a work-function of n+ Si, the channel region comprising respective portions below each gate electrode region.

26. (Previously presented) The pixel cell of claim 25, wherein each gate electrode region extends over an active area by a different distance.

27. (Currently amended) A pixel cell comprising:

a photo-conversion device at a surface of a substrate; and

a transistor formed over a substrate and adjacent to the photo-conversion device, the transistor comprising a gate electrode overlying a channel region and having a length extending from a source/drain region to the photo-conversion device, the gate electrode comprising first, second, and third gate electrode regions and each gate electrode region extending the length of the gate electrode, wherein the first gate electrode region is between the second and third gate electrode regions, and wherein the second and third gate electrode regions are over an area where an isolation region and an active region meet, and wherein at least one of the second and third gate electrode regions has a work-function greater than a work-function of n+ Si, the channel region comprising first, second, and third portions below each gate electrode region, respectively.

28. (Previously Presented) The pixel cell of claim 27, wherein the second and third gate electrode regions have a same work-function.

29. (Previously Presented) The pixel cell of claim 27, wherein a doping concentration of at least one of the second and third channel portions is determined at least in part by the work-function of the respective gate electrode region.

30. (Currently amended) An image sensor, comprising:

an array of pixel cells, wherein each pixel cell comprises:

a photo-conversion device,

a floating diffusion region, and

a transistor for gating charge from said photo-conversion device to said floating diffusion region, said transistor comprising a gate electrode having a length ~~and a width,~~ and a channel region under said gate electrode,

said ~~width~~ length of said gate electrode extending from said photo-conversion device to said floating diffusion region,

said length of said gate electrode being divided into a plurality of gate electrode regions, each gate electrode region extending from said photo-conversion device to said floating diffusion region, wherein at least one said gate electrode region has a work-function greater than a work-function of n+ Si, and another said gate electrode region has a different work-function from that of said at least one gate electrode region, said channel region comprising respective portions below each gate electrode region, wherein a doping concentration of at least one portion of said channel region is determined in part by the work-function of the respective gate electrode region.

31. (Original) The image sensor of claim 30, wherein the image sensor is a CMOS image sensor.

32. (Original) The image sensor of claim 30, wherein the image sensor is a charge coupled device image sensor.

33. (Previously presented) The image sensor of claim 30, wherein the transistor is a transfer transistor.

34. (Previously presented) The image sensor of claim 30, wherein at least one gate electrode region comprises a mid-gap material.

35. (Original) The image sensor of claim 34, wherein the mid-gap material is selected from the group consisting of: $Si_{1-x}Ge_x$, TiN/W, Al/TiN, TifFiN, and TaSiN.

36. (Original) The image sensor of claim 35, wherein the mid-gap material is $Si_{1-x}Ge_x$, and wherein the mole fraction of Ge in $Si_{1-x}Ge_x$ is approximately 0.4.

37. (Previously presented) The image sensor of claim 36, wherein the least one gate electrode region is doped to one of a first or second conductivity type.

38. (Previously presented) The image sensor of claim 30, wherein at least one gate electrode region comprises a degenerately doped p+ polysilicon layer.

39. (Previously presented) The image sensor of claim 30, wherein at least one gate electrode region comprises a layer of lower doped polysilicon of a first or second conductivity type.

40. (Previously presented) The image sensor of claim 39, wherein the at least one gate electrode region has a dopant profile allowing for at least partial depletion of the at least one gate electrode region.

41. (Original) The image sensor of claim 30, wherein there is approximately no active dopant in at least one portion of the channel region.

42. (Currently amended) The image sensor of claim 30, wherein the at least one said gate electrode region is a first gate electrode region and the another said gate electrode region is a second gate electrode region and the transistor comprises ~~first and~~

~~second gate electrode regions and~~ first and second channel portions below the first and second gate electrode regions, respectively.

43. (Previously presented) The image sensor of claim 42, wherein the first and second gate electrode regions each extend over an active area by a different distance.

44. (Previously presented) The image sensor of claim 42, wherein the first and second gate electrode regions have different work-functions, and wherein each work-function is greater than a work-function of n+ Si.

45. (Currently amended) The image sensor of claim 30, wherein the at least one said gate electrode region is a first gate electrode region and the another said gate electrode region is a second gate electrode region and the first transistor comprises ~~first, second, and~~ a third gate electrode regions extending from said photo-conversion device to said floating diffusion region and first, second, and third channel portions below the first, second, and third gate electrode regions, respectively.

46. (Original) The image sensor of claim 45, wherein the first gate electrode region is between the second and third gate electrode regions, and wherein the second and third gate electrode regions are each over a respective area where an isolation region and an active region meet, and wherein at least one of the second and third gate electrode regions has a work-function greater than a work-function of n+ Si.

47. (Original) The image sensor of claim 46, wherein the second and third gate electrode regions have a same work-function.

48. (Original) The image sensor of claim 46, wherein the doping concentration of at least one of the second and third channel portions is determined at least in part by the work-function of the respective gate electrode region.

49. (Currently amended) A processor system, comprising:

(i) a processor; and

(ii) an image sensor coupled to the processor, the image sensor comprising:

a pixel comprising:

a photo-conversion device,

a sensing node, and

a transistor for gating charge from said photo-conversion device to said sensing node, said transistor comprising a gate electrode having a length ~~and a width,~~ and a channel region under said gate electrode,

said ~~width~~ length of said gate electrode extending from said photo-conversion device to said sensing node,

the length of said gate electrode being divided into two gate electrode regions, each gate electrode region extending from said photo-conversion device to said sensing node, wherein one said gate electrode region has a work-function greater than a work-function of n+ Si, and another said gate electrode region has a different work-function from that of said one gate electrode region, said channel region comprising respective portions below each gate electrode region, wherein a doping concentration of at least one portion of said channel region is determined in part by the work-function of the respective gate electrode region.

50. (Original) The system of claim 49, wherein the image sensor is a CMOS image sensor.

51. (Original) The system of claim 49, wherein the image sensor is a charge coupled device image sensor.

52. (Currently amended) A method of forming a pixel cell, the method comprising:

forming a photo-conversion device;

forming a sensing node; and

forming a first transistor for gating charge from said photo-conversion device to said sensing node; the act of forming said first transistor comprising forming a gate electrode having a length ~~and a width,~~ and forming a channel region under said gate electrode,

said ~~width~~ length of said gate electrode extending from said photo-conversion device to said sensing node,

said length of said gate electrode being divided into a plurality of gate electrode regions, each gate electrode region extending from said photo-conversion device to said sensing node, wherein at least one said gate electrode region has a work-function greater than a work-function of n+ Si, and another said gate electrode region has a different work-function from that of said at least one gate electrode region, the act of forming said channel region comprising forming at least one channel portion under said at least one gate electrode region.

53. (Original) The method of claim 52, wherein the act of forming the first transistor comprises forming a transfer transistor for transferring photo-generated charge from the photo-conversion device to a floating diffusion region.

54. (Previously Presented) The method of claim 52, wherein at least one gate electrode region comprises forming a layer of mid-gap material.

55. (Original) The method of claim 54, wherein the act of forming the layer of mid-gap material comprises forming the layer of mid-gap material selected from the group consisting of: $Si_{1-x}Ge_x$, TiN/W, Al/TiN, Ti/TiN, and TaSiN.

56. (Original) The method of claim 55, wherein the act of forming a layer of mid-gap material comprises forming a layer of $Si_{1-x}Ge_x$, wherein a mole fraction of Ge is approximately 0.4.

57. (Original) The method of claim 56, wherein the act of forming a layer of $Si_{1-x}Ge_x$ comprises doping the layer of $Si_{1-x}Ge_x$ to one of a first or second conductivity type.

58. (Previously Presented) The method of claim 52, wherein at least one gate electrode region comprises forming a layer of degenerately doped p+ polysilicon.

59. (Previously Presented) The method of claim 52, wherein at least one gate electrode region comprises forming a layer of lower doped polysilicon of a first or second conductivity type.

60. (Previously Presented) The method of claim 59, wherein the act of forming the layer of lower doped polysilicon comprises forming the layer of lower doped polysilicon having a dopant profile allowing for at least partial depletion of the at least one gate electrode region.

61. (Original) The method of claim 60, wherein the act of forming the layer of lower doped polysilicon comprises doping the polysilicon with indium.

62. (Original) The method of claim 52, wherein forming the channel region comprises forming at least one portion of the channel region having approximately no active dopant concentration.

63. (Currently Amended) The method of claim 52, wherein the act of forming the gate electrode comprises forming the at least one said gate electrode region as a first gate electrode region and forming the another said gate electrode region as a second gate electrode regions, and wherein the act of forming the channel region comprises forming first and second channel portions below the first and second gate electrode regions, respectively.

64. (Previously presented) The method of claim 63, wherein the act of forming the first and second gate electrode regions comprises forming the first and second gate electrode regions such that each of the first and second gate electrode regions extends over an active area by a different distance.

65. (Previously presented) The method of claim 63, wherein the first and second gate electrode regions are each formed having different work-functions, each work-function being greater than a work-function of n+ Si.

66. (Currently Amended) The method of claim 52, wherein the at least one said gate electrode region is a first gate electrode region and the another said gate electrode region is a second gate electrode region and the act of forming the gate electrode comprises forming ~~first, second, and~~ a third gate electrode regions, and wherein the act

of forming the channel region comprises forming first, second, and third channel portions below the first, second, and third gate electrode regions, respectively.

67. (Previously presented) The method of claim 66, wherein the first gate electrode region is formed between the second and third gate electrode regions, and wherein the second and third gate electrode regions are each formed over a respective area where an isolation region and an active region meet, and wherein at least one of the second and third gate electrode regions has a work-function greater than a work-function of n+ Si.

68. (Previously presented) The method of claim 67, wherein the second and third gate electrode regions are formed having a same work-function.

69. (Previously presented) The method of claim 67, wherein the act of forming the second and third channel portions comprises forming the second and third channel portions such that a doping concentration of at least one of the second and third channel portions is determined at least in part by the work-function of the respective gate electrode region.

70. (Previously presented) The method of claim 52, further comprising:

forming a second transistor, the act of forming the second transistor comprising forming at least one second transistor gate electrode region having a work-function greater than a work-function of n+ Si.

71. (Previously presented) The method of claim 70, wherein the at least one second transistor gate electrode region is formed of the same material as the at least one gate electrode region.

72. (Canceled)

73. (Previously presented) A method of forming a pixel cell, the method comprising:

forming a photo-conversion device; and

forming a transistor adjacent to the photo-conversion device, the act of forming the transistor comprising forming a gate electrode overlying a channel region, the act of forming the gate electrode comprising forming a gate electrode having a length extending from a source/drain region to the photo-conversion device, the gate electrode comprising at least two gate electrode regions, each gate electrode region extending the length of the gate electrode and having a substantially uniform dopant type and concentration, wherein at least one of the gate electrode regions has a work-function greater than a work-function of n+ Si, the act of forming the channel region comprising forming respective portions below each gate electrode region.

74. (Previously presented) The method of claim 73, wherein the act of forming the at least two gate electrode regions comprises forming each of the gate electrode regions extending over an active area by a different distance.

75. (Currently amended) A method of forming a pixel cell, the method comprising:

forming a photo-conversion device at a surface of a substrate; and

forming a transistor adjacent to the photo-conversion device, the act of forming the transistor comprising forming a gate electrode overlying a channel region, the act of forming the gate electrode comprising <u>forming a gate electrode having a length</u>

extending from a source/drain region to the photo-conversion device, and forming first, second, and third gate electrode regions, each gate electrode region extending the length of the gate electrode and wherein the first gate electrode region is formed between the second and third gate electrode regions, and wherein the second and third gate electrode regions are each formed over a respective area where an isolation region and active region meet, and wherein at least one of the second and third gate electrode regions is formed having a work-function greater than a work-function of n+ Si, the act of forming the channel region comprising forming first, second, and third portions below the first, second, and third gate electrode, regions, respectively.

76. (Previously Presented) The method of claim 75, wherein the second and third gate electrode regions are formed having a same work-function.

77. (Previously Presented) The method of claim 75, wherein the doping concentration of at least one of the second and third channel portions is determined at least in part by the work-function of the respective gate electrode region.

The following is an examiner's statement of reasons for allowance:

Examiner notes that the Figure shown in Remarks filed 06/11/07 is confusing because it labels the length and the width of the gate electrode in a manner that goes away from the conventional interpretation of the art and this application's specification. The Figure in the Remarks filed (05/08/07) shows the length of a gate electrode in the properly defined manner. This discrepancy between the length and width of the gate electrode interpretation has been clarified with regard to claim 1 in the examiner's amendment.

The prior art of record fails to anticipate or render obvious the claim limitations including a plurality of gate electrode regions extending from a photo-conversion device to one of a source/drain region, a sensing node, and a floating diffusion region with a gate electrode region having a work-function greater than a work-function of n+ Si.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Election/Restrictions

Claims 1-23, 25-71 and 73-77 are allowable. The restriction requirement between species, as set forth in the Office action mailed on 09/01/2004 and 12/14/2004, has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). **The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.** Claim 14-23, 25-29, 42-48, 63-71 and 73-77 are directed to a plurality of gate electrode regions extending from a photo-conversion device to one of a source/drain region, a sensing node, and a floating diffusion region are no longer withdrawn from consideration because the claim(s) requires all the limitations of an allowable claim.

In view of the above noted withdrawal of the restriction requirement, applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is 571-272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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09/04/07

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